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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,692	01/30/2004	Andrew M. Spencer	10015022-1	8610

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,692	SPENCER ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,19,22-27* is/are rejected.

7)☒ Claim(s) *13-18,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/2004*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *10022006* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steve Dicke (Reg #: 38,431) on 10 February 2006.

Claims 19 and 22 are modified to be dependent on claim 9, not on claim 8, so that the preambles of both claims now reads as "The system-on-a-chip of claim 9, wherein the memory controller further comprises: ".

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7 and 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As for claim 7, it is unclear to one ordinarily skilled in the art how it is possible for the non-volatile semiconductor imperfect memory to be comprised in the system-on-a-chip while being external to the system-on-a-chip at the same. Appropriate corrections are required.

As for claim 27, if the system-on-a-chip and the semiconductor are the same semiconductor chip, then it is unclear to one ordinarily skilled in the art how a memory device can be comprised within a system-on-a-chip, while still enables communication between with the same system-on-a-chip which includes itself, and itself. Appropriate corrections are required.

Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As for claim 27, the only way for the claim to avoid a rejection under 35 U.S.C. 112, first paragraph for failure to comply with the enablement requirement, is to interpret the claim as describing two different semiconductors. However, the specification does not disclose such two different semiconductors. Appropriate corrections are required.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 8 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, it is unclear what exactly is defined as "device data" in the Application. Is it some device configuration data, or just data of a device? The Examiner is rejecting the claim in view of the second interpretation. Appropriate correction is required.

As for claims 8 and 24, the exact meaning of the phrase "a memory controller configured to receive at least one data block from the microprocessor using an associated logical block address" is unclear to the Examiner. Is the data block received using the logical block address, or is it received from a microprocessor that uses logical

block address? Or are both true? The Examiner is rejecting the claims in view of the first interpretation.

As for claims 8 and 24, the exact meaning of the phrase "to send the at least one data block and error correction code to the non-volatile semiconductor-based imperfect memory device using the physical block address" is unclear to the Examiner. Is the data block and error correction code sent using the physical block address, or are they sent to a memory device that uses the physical block address? Or are both true? The Examiner is rejecting the claims in view of the first interpretation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 4, 8, 9, 11, 12, 22, 23, 24, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. [US 6,317,371 B2] (hereinafter "Katayama"), in further view of Hauck [US 6,961,807 B1] (hereinafter "Hauck").

As for claims 1, 2, 3, 4, 8, 24, and 27, Katayama teaches a microprocessor (Col 9, Lines 53-55; the personal computer/host must have at least one microprocessor) and a system-on-a-chip (Col 20, Lines 55-63), the system-on-a-chip comprising:

a non-volatile semiconductor-based imperfect memory device (Fig 1, 1 Electrical Reloadable ROM; Fig 6, 52 Electrically Reloadable ROM; Col 9, Lines 6-18; Col 14, Lines 23-25); and

a memory controller (Fig 6, 51 Controller) configured to receive at least one data block from the microprocessor using an associated logical block address (Col 14, Lines 24-27; Col 14, Lines 32-40; Col 14, Lines 55-60; Col 15, Lines 46-67; Col 16, Lines 1-14), to translate the associated logical block address to a corresponding physical block address (Col 17, Lines 1-25; Col 9, Lines 66-67; Col 10, Lines 1-7; Col 11, Lines 41-67; Col 12, Lines 1-7), to provide for the at least one data block an error correction code that is a function of the at least one data block (Col 15, Lines 9-20; Col 16, Lines 1-14; Fig 7, 66 Data Region ECC), to send the at least one data block and error correction code to the non-volatile semiconductor-based imperfect memory device using the physical block address (Col 16, Lines 1-14; Col 17, Lines 1-25), and to provide error detection and correction for the at least one data block based on the at least one data block and error correction code read from the non-volatile semiconductor-based imperfect memory device (Col 16, Lines 21-37).

Katayama further teaches that the Memory Controller and the non-volatile imperfect semiconductor memory device are in a system-on-a-chip to reduce the scale of the circuitry (Col 20, Lines 55-63), but does not specifically disclose that the

microprocessor is also in the system-on-a-chip. However, Hauck teaches a system-on-a-chip device comprising a controller, a memory, and a microprocessor (Hauck: Fig 3, 20 Die, 60 Package) in order to further reduce circuitry scale according to the same principle described by Katayama. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to further include Katayama's microprocessor in the system-on-a-chip of Katayama, in order to reduce circuitry scale.

It is clear that the system-on-a-chip described by claims 1-4 are already substantially described by the system-on-a-chip of claim 8.

It is also clear that the system-on-a-chip of claim 24 is substantially described by the system-on-a-chip of claim 8, and it is comprised within a mobile electronic device (Fig 6, 50 flash memory card is a mobile electronic device as it can be attached and detached to the 5 system bus; Col 14, Lines 17-22; Lines 57-60), and the method of claim 27 is performed by the system-on-a-chip described by claims 8 and 24.

As for claim 9, the combined references of Katayama and Hauck teach the memory controller further comprises:

a buffer memory configured to receive a plurality of data blocks (Fig 6, the combination of 59 Data Buffer 1 and Data Buffer 2), including the at least one data block, from the microprocessor and to send the plurality of data blocks to the non-

volatile semiconductor-based imperfect memory device (Col 14, Lines 65-67; Col 15, Lines 1-8; Col 15, Lines 65-67; Col 16, Lines 1-13); and

a buffer manager (Fig 6, combination of 57 If/Control Circuit, 63 CPU, 58 Data Transfer Control Circuit, 61 host side switching circuit, 62 memory buffer side switching circuit) comprising:

a hardware-implemented logic block configured to manage the transfer of the plurality of data blocks between the microprocessor and the non-volatile semiconductor-based imperfect memory device (Fig 6, combination of 57 If/Control Circuit, 63 CPU, 58 Data Transfer Control Circuit, 61 host side switching circuit, 62 memory buffer side switching circuit), wherein the buffer manager enables the microprocessor to access a first data block at a first location within the buffer memory while a second data block is concurrently being written to the non-volatile semiconductor-based imperfect memory device from a second location within the buffer memory (Col 16, Lines 37-41; Col 4, Lines 57-65); and

a memory mapping block configured to receive from the non-volatile semiconductor-based imperfect memory device a memory map indicating reserved memory locations within the non-volatile semiconductor-based imperfect (Col 6, Lines 20-52; Col 10, Lines 56-67; Col 11, Lines 1-3; Col 18, Lines 54-67; Fig 8; Fig 9) and comprising:

a hardware-implemented logic block configured to translate a logical block address to a corresponding physical block address based upon the memory map (Col 17, Lines 1-25; Fig 8; Fig 9).

As for claim 11, Katayama further teaches the buffer memory comprises a number of bit positions wherein the number of bit positions is a multiple of a number of bit positions in the at least one data block (Fig 6, the combination of 59 Data Buffer 1 and Data Buffer 2 of the memory buffer is capable of storing two data blocks of 53 Stored Data; Col 14, Lines 65-67; Col 15, Lines 1-8).

As for claim 12, Katayama further teaches the number of buffer memory bit positions is a multiple of 512 (Col 9, Lines 22-24; Col 14, Lines 33-37; each data block is 512 bytes, and the memory buffer is capable of storing two data blocks as described in claim 11).

As for claim 22, it is clear the claim is already substantially disclosed as described above, with the memory interface of the instant claim comprising 58 Data Transfer Control Circuit, 63 CPU, 61 host side switching circuit, 62 memory buffer side switching circuit, IF/Control Circuit, 55 DATA ECC Circuit, 56 Administrative ECC Circuit, and buffers 59 and 60 of Figure 6.

As for claim 23, the memory interface described above is implemented in hardware (Fig 6, 58 Data Transfer Control Circuit, 63 CPU, 61 host side switching circuit, 62 memory buffer side switching circuit, IF/Control Circuit, 55 DATA ECC Circuit, and 56 Administrative ECC Circuit; also the buffers 59 and 60 must be hardware).

Claims 5 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama [US 6,317,371 B2] and Hauck [US 6,961,807 B1], in further view of Gibson et al. [5,557,596] (hereinafter "Gibson").

As for claims 5 and 25, the claim is already substantially disclosed as described above, but the combined teaching of Katayama and Hauck does not teach that the memory device is an ultra-high density atomic resolution memory device. However, Gibson teaches that an ultra-high density atomic resolution memory device possesses the attributes of higher storage density, lower storage cost, faster access time and higher data rate than other information storage devices such as magnetic hard-drives, optical drives, and DRAM (Col 1, Lines 10-56). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use an ultra-high density atomic resolution memory device as the memory device of the combined teaching of Katayama and Hauck, in order to have higher storage density, lower storage cost, faster access time, and higher data rate.

Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama [US 6,317,371 B2] and Hauck [US 6,961,807 B1], in further view of Bhattacharyya [US 6,466,471 B1] (hereinafter "Bhattacharyya").

As for claims 6 and 26, the claim is already substantially disclosed as described above, but the combined teaching of Katayama and Hauck does not teach that the memory device is a magnetic random access memory device. However, Bhattacharyya teaches that a magnetic random access memory device is a non-volatile memory that possesses the attributes of much faster data access time than conventional long term storage devices such as hard drives, smaller size, and less power consumption (Col 1, Lines 10-16). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a magnetic random access memory device as the memory device of the combined teaching of Katayama and Hauck, in order to have faster data access time, smaller size, and less power consumption.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama [US 6,317,371 B2] and Hauck [US 6,961,807 B1], in further view of Bell [5,410,707] (hereinafter "Bell").

As for claim 7, the claim is already substantially disclosed as described above, but the combined teaching of Katayama and Hauck does not teach that the memory device is external to the system-on-a-chip. However, Bell teaches that using an external memory for data storage possesses the attributes of detachability for replacement and mobility (Col 3, Lines 43-54; Col 4, Lines 9-28). Therefore, it would

have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a memory device external to the system-on-a-chip as the memory device of the combined teaching of Katayama and Hauck, in order to have detachability for replacement and mobility.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama [US 6,317,371 B2] and Hauck [US 6,961,807 B1], in further view of Storm et al. [5,884,067] (hereinafter "Storm").

As for claim 10, the claim is already substantially disclosed as described above, but the combined teaching of Katayama and Hauck does not teach that the buffer memory is configured as a circular buffer. However, Storm teaches a circular buffer in a memory controller which possesses the attributes of reducing the frequency with which the data bus must stall while waiting for the memory module bus to clear when data is to be written to the memory when the buffer is used with a multi-processor system. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a circular buffer as the buffer memory of the combined teaching of Katayama and Hauck, in order to reduce bus stall frequency when used with a multi-processing system.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama [US 6,317,371 B2] and Hauck [US 6,961,807 B1], in further view of Wu et al. [US 6,917,967 B2] (hereinafter "Wu").

As for claim 19, the claim is already substantially disclosed as described above, but the combined teaching of Katayama and Hauck does not teach that the memory translator comprises a hardware-implemented logic block configured to synchronize a transfer of the plurality of data blocks between the buffer memory and the non-volatile semiconductor-based imperfect memory device. However, Wu teaches that a hardware-implemented logic block (Fig 8, 10A and 10B must be hardware-implemented) which synchronizes data access and transfer of storage devices which are shared resources in order to enforce synchronization on the accesses of the shared resource so that they are accessed in a deterministic fashion (Col 14, Lines 25-67; Col 15, Lines 1-52). Since the buffer memory of Katayama and Hauck's combined teaching is also a shared resource, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a hardware-implemented logic block in the translator of the combined teaching of Katayama and Hauck, in order to synchronize the accesses to the buffer memory in a deterministic fashion.

Allowable Subject Matter

Claims 13-18, 20, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 13 is allowable as the combined teachings of Katayama and Hauck disclose the buffer manager configured to received a plurality of data blocks from the microprocessor, but none of the cited references teach that the plurality of data blocks are set-up information blocks comprising information to enable transfer of the plurality of data blocks between the microprocessor and the non-volatile semiconductor-based imperfect memory device.

Claims 14-18 are allowable as they are dependent on claim 13 and contain further allowable subject matter.

Claim 20 is allowable as the combined teachings of Katayama, Hauck, and Wu disclose the hardware-implemented logic block to synchronize the transfer of the plurality of data blocks between the microprocessor and the buffer memory, but none of the cited references teaches that the microprocessor transfers data at a first bit-width and the buffer memory transfers data at a second bit-width, and the logic block comprises a plurality of buffers to synchronize the transfers.

Claim 21 is allowable as the combined teachings of Katayama, Hauck, and Wu disclose the hardware-implemented logic block to synchronize the transfer of the plurality of data blocks between the microprocessor and the buffer memory, but none of

the cited references teaches that the microprocessor transfers data at a first data rate and the buffer memory transfers data at a second data rate, and the logic block comprises a plurality of buffers to synchronize the transfers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

2/20/03
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

14 February 2006